10-06-00

A

PATENT
SNR Matter No.09785980-0021
00CXT0319T

Box PATENT APPLICATION
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Date: October 3, 2000

Docket No. 09785980-0021

Sir:

Transmitted herewith for filing is the patent application of

Inventors: Richard A. Mann and Lester J. Kozlowski

For: CMOS IMAGER WITH DISCHARGE PATH TO SUPPRESS RESET NOISE

I hereby certify that this paper is being deposited with the United States Postal Service as Express Mail in an envelope addressed to: Assistant Commissioner For Patents, Washington, D.C. 20231, on this date

10-5-00
Date

Shirley Tom

Express Mail Label No. EI164225168US

Enclosed are:

- ☒ 12 pages of specification, 7 pages of claims and an abstract.
- ☒ an executed oath or declaration, with power of attorney.
- ☐ an unexecuted oath or declaration, with power of attorney.
- ☐ ___ sheet(s) of informal drawing(s).
- ☒ 7 sheets of formal drawings.
- ☒ Assignment of the invention to Conexant Systems, Inc.
- ☐ Assignment Form Cover Sheet.
- ☐ A check in the amount of $_____ to cover the fee for recording the assignment(s) is enclosed.
- ☐ Associate power of attorney.

Fee Calculation For Claims As Filed

a) Basic Fee							$	710.00
b) Independent Claims	3	- 3 =	0	X	$80.00	=	$	0.00
c) Total Claims	49	- 20 =	29	X	$18.00	=	$	522.00
d) Fee for Multiple Claims			0	X	$260.00	=	$	0.00
					Total Filing Fee		$	1,232.00

- ☐ Statement(s) of Status as Small Entity, reducing Filing Fee by half to $
- ☐ Check No. in the amount of $ to cover the filing fee is enclosed
- ☒ Charge $ 1,272.00 to Deposit Account No. 500835 for the basic filing fees of $1,232.00 and $40.00 for recording the enclosed assignment.
- ☐ Other _____.
- ☒ The Commissioner is hereby authorized to charge any additional fees which may be required to this application under 37 C.F.R. §§1.16-1.17, or credit any overpayment, to Deposit Account No. 500835. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 500835. Two duplicate copies of this sheet are enclosed.

Francisco A. Rubio-Campos
SONNENSCHEIN NATH & ROSENTHAL
P. O. Box #061080
Wacker Drive Station, Sears Tower
Chicago, Illinois 60606-1080
(312) 876-8000

By: _____
Francisco A. Rubio-Campos
Registration No. 45,358

Express Mail" Mailing No.: EI16422516SUS

Date of Deposit: October 5, 2000

PATENT
SNR Matter No.09785980-0021
00CXT0319T

TAPERED THRESHOLD RESET FET FOR CMOS IMAGERS

INVENTORS

Richard A. Mann
Lester J. Kozlowski

BACKGROUND OF THE INVENTION

1. Technical Field.

This invention relates to electronic imaging devices and, in particular, to imagers having FET reset switches.

2. Related Art.

Conventionally, CMOS imagers contain a number of photodiodes that are continuously queried and reset. The resetting of the photodiodes attempts to place each of the photodiodes into a known state (i.e. an expected voltage or charge level) and is commonly controlled by a N-channel Metal Oxide Semiconductor (NMOS) Field Effect Transistor (FET) acting as a reset switch. The NMOS FET has a drain implant that is in direct contact with a lighter doped P-well and protrudes into the material under the gate region of the NMOS FET.

The utilization of NMOS FETs acting as reset switches in CMOS imagers results in an additional source of noise, commonly known as reset noise (known as kTC noise). The typical construction of a NMOS FET allows charge to flow back to the drain and contributes to the reset noise in a CMOS imager. The length of time between resets and temperature changes affects the rate at which charge in a NMOS FET flows back to the drain and increases the reset noise when voltage is removed from the gate. The problem created by reset noise in a CMOS imager is that it causes uncertainty about the voltage values at the photodiodes after a reset. Attempts to compensate for

reset noise in a NMOS FET have been generally unsuccessful due to charge redistribution that depends on the localized substrate noise (i.e. correlated double sampling measurements of the reset noise during a read operation). In addition, for signal readout circuits configured to integrate the photogenerated signal on the total sense capacitance, such as the source follower arrangement of Fry, *et al.*, (IEEE JSSC, Vol. SC-5, No. 5, October 1970), is affected by the increased capacitance. The increased capacitance of a conventional reset FET decreases the electrical gain of the signal readout circuits. The decreased electrical gain results from the sense capacitance being the aggregate of the detector capacitance and various stray capacitances in compact pixel designs. The stray capacitances include, for example, the gate capacitance of the transistor gate driven by the photodiode cathode and the associated capacitance of the reset transistor. Therefore, the increased capacitance of a conventional NMOS FET reset switch results in optical degraded sensitivity for the CMOS imager due to both higher reset noise and lower electro-optical sensitivity. Thus, the use of known types of compensation for reset noise still results in a loss of sensitivity in the CMOS imager.

Additional reset noise problems occur due to the single chip construction of a conventional NMOS FET utilized as a reset switch in a CMOS imager. Construction of conventional NMOS FET utilize fabrication methods using sub-micron technology. As a result, the NMOS FET is susceptible to junction leakage. It is not uncommon for high leakage to occur from the increased electric field associated with a shallow junction, Arsenic implant damage, gate induced drain leakage, or a combination of all of the previous. The junction leakage of a conventional NMOS FET results in poor optimization and continuous soft resets during low light operation of a CMOS imager.

Soft resets generate image lag because the charge that is not fully cleared from the photo-detector is subsequently added to the signal in the next integration period. The poor optimization and continuous soft resets significantly contributes to the reset noise and loss of sensitivity at low light level problems in a CMOS imager. Therefore, there is a need for a device and method to increase sensitivity at low light level while reducing the reset noise in CMOS imagers regardless of temperature and periods between resets of photodiodes while reducing junction leakage of the NMOS FET.

SUMMARY

The tapered threshold reset FET for a CMOS imager has a sensor having a transistor with a gate located partially over a source and partially over a drain having material between the source and drain beneath the gate of a predetermined length. The sensor also has a detection device that may be coupled to the drain by a signal path, where the material allows the detection device to be reset to a predetermined state.

Broadly conceptualized, the sensor may be formed with a reset transistor that reduces the capacitance of the photodiode. This may be accomplished by moving the p-type well, that isolates the source from the drain such that the p-type well partially dopes the channel of the transistor. The transistor may also be constructed to reduce reset noise through the use of the tapered reset operation. The tapered reset operation may include a reset transistor of relatively high impedance capable of suppressing the basic reset noise associated with the photodiode capacitance via an on-chip circuit and by using a channel implant that increases the reset voltage level for creating the reset channel.

Other systems, methods, features and advantages of the invention will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods features and advantages be included within this description, be within the scope of the invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE FIGURES

The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principals of the invention. In the figures, like reference numerals designate corresponding parts throughout the different views.

FIG. 1 is a schematic diagram depicting an exemplary implementation of a sensor having a photo-detector and a reset switch in accordance with the invention.

FIG. 2 is a cross sectional view illustrating the sensor of FIG. 1 having a FET transistor reset switch.

FIG. 3 is a cross sectional view illustrating another example of the sensor of FIG. 1 having a FET transistor reset switch.

FIG. 4 is a cross sectional view illustrating still another exemplary implementation the sensor of FIG. 1 having a FET transistor.

FIG. 5 is a flow diagram illustrating an example process for resetting the sensor of FIG. 4.

FIG. 6 is a signal diagram illustrating a tapered reset voltage applied to the FET of FIG. 4.

FIG. 7 is a flow diagram illustrating example process for resetting the sensor of FIG. 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In FIG. 1, a schematic diagram depicting a sensor 100 having a photo-detector 102 and a transistor 104 acting as a reset switch is shown. The sensor 100 includes a photo-detector 102 having of a p-n junction and the transistor 104 acting as a reset switch. The transistor has a source 106, a gate 108, and a drain 110. The gate 108 of transistor 104 is electrically connected to a reset voltage supply 112. The source 106 of transistor 104 is electrically connected to a reset voltage sink 114, preferably ground. The drain 110 of transistor 104 is electrically connected to the anode 116 of the photo-detector 102 and a readout circuit 118. The readout circuit 118 samples and processes the output of the photo-detector 102 during a read operation of the sensor 100. However, one skilled in the art appreciates, that in an alternate embodiment the photo-detector may selectively be electrically associated with the source 106 as opposed to the drain 110 to facilitate a reset of the photo-detector 102.

Upon a reset voltage being applied to the gate 108 of transistor 104 (acting as a reset switch) via the reset voltage supply 112, a positive charge on the photo-detector 102 passes from the drain 110 to the source 106 of transistor 104 and ultimately to the reset voltage sink 114. Once the reset operation is complete and the transistor 104 is turned off (i.e. the voltage on the gate 108 is removed), the remaining charge on the photo-detector 102 is measured and stored in memory (not shown) via readout circuit 118. The stored charge value is utilized for correlated double sampling (CDS) in order to reduce reset noise via post processing and is a measure of offset error including the offset associated with the readout circuit 118 amplification, the random offsets generated by charge redistribution, and the classical reset noise. The offset error is described by the expression:

$$reset\ noise\ (carriers) = \frac{\sqrt{kTC_{sense}}}{e}$$

where "k" is Boltzman's constant, "T" is the temperature, "C_{sense}" is the sense capacitance and "e" is the electron charge. In FIG. 1, C_{sense} is comprised of the capacitance of photodiode 102, the input capacitance of the readout circuit 118, and the stray capacitance associated with the transistor 104 acting as a reset switch. Minimizing the capacitances reduces the maximum reset noise in sensor 100 with out utilizing the additional hardware and costs associated with CDS.

Radiation or light is then permitted to accumulate on the photo-detector 102 for a predefined time (i.e. integration period), before the charge is read again via the readout circuit 118. Ideally, the error in this second read is corrected by compensating for the earlier measurement for offset and reset noise. The reset error, however, may be significant and vary depending on the length of time of the reset and the construction of transistor 104 utilized as the reset switch.

FIG. 2 is an illustration of a cross sectional view of the sensor100. The sensor 100 has a photo-detector 102, a FET transistor 104 reset switch. The transistor 104 has a gate 108 with a dielectric insulator 200, a source 106, and a drain 110 formed in a substrate 202. The source 106 is formed within a p-type well 204 (p-type atoms include Phosphorus, Arsenic, Nitrogen Antimony, and Bismuth) and is partially beneath the gate 108. The p-type well 204 is implanted or formed within the substrate 202. The source 106 is preferably formed as a shallow surface implant on the p-type well 204. The drain 110 is preferably formed with the substrate 202 to be partially beneath the gate 108. The drain 110 is electrically associated with a photo-detector 102 formed with the surface implant of the drain 110, deep implant 210, and substrate 202.

Additionally, a person skilled in the art would recognize that the source 106 may selectively be interchanged with the drain 110 and associated with the photo-detector 102.

The transistor 104 of sensor 100 further includes a material in the space defined by the separation of the source 106 from the drain 110 beneath the gate 108. In an example implementation of the transistor 104, the length 206 of the material is at least 20 percent longer than a process minimum. For example, the process minimum gate length for a conventional 3.3 volt logic process range is approximately 0.35 microns. The recommended minimum gate length to avoid exaggerated short channel effects would be approximately 0.4 microns. While increasing the length 206 of the material consumes additional die area, increasing the material length 206 by approximately 20 percent of the process minimum increases the potential required to deplete the reset channel. But, the increase in potential required to deplete the reset channel significantly decreases the likelihood of a soft reset during a read operation (i.e. sub-threshold leakage does not degrade low light operation) and promotes the proper functioning of the various forms of tapered reset. An additional result of increasing the length of the gate 108 is that the doping of the gate 108, source 106, drain 110, and associated channel may be decreased.

The channel has a well portion and a shallow implant 208. The implant 208 may be formed with a Boron dopant, but other implementations may selectively utilize hole-increasing dopants such as Aluminum, Gallium, Indium, and Thallium. The well portion of the channel constitutes a portion of the p-type well 204. The implant 208 is disposed between the channel well portion 204 of the source 106 and the drain 110. Additionally, one skilled in the art would appreciate, the channel implant 208 may be

disposed between the channel well portion and the source 106 when the photo-detector 102 is formed to be operably associated with the source 106.

The implant 208 is preferably formed to be sufficiently shallow such that the concentration of dopant near the channel surface under the gate 108 further increases the potential that must be applied to the gate 108 in order to deplete the reset channel and the implant 208 dose may be reduced to below the dopant level of the channel well portion. In this instance, because the implant 208 has a lower dopant level than the channel well portion, the drain 110 dose may be advantageously reduced from $3e^{13}$ cm^{-3} n-type, the typical level for a conventional NMOS FET, to approximately $6e^{12}$ cm^{-3} n-type. This has the additional advantage of reducing the capacitance of the photo-detector 102 relative to its volume and lowering junction leakage associated with arsenic implant damage and gate 108.

In FIG. 3, a cross sectional view of an exemplary implementation of the sensor 300 of FIG. 1 is illustrated. The FET transistor 302 has a gate 304, a source 306, and a drain 308. The drain 308 of the transistor 302 is connected to the deep implant 316 of photo-detector 310. The gate 304 has a n-type region 312, a p-type region 314, and a dielectric insulator 316. The source 306 includes a p-type well 318 located in a substrate 320. In this implementation, material is located between the p-type well 318 of the source 306 and the drain 308. The length 322 of the material is defined by the separation of the source 306 from the drain 308 beneath the gate 304. The length 322 of the material is preferably at least 20 percent longer than the process minimum.

As depicted in FIG. 3, the gate 304 has an n-type region 312, and a p-type region 314 that form gate 304. The gate 304 is preferably formed with polysilicon regions of opposite polarity (examples of polysilicons are; Boron, Aluminum, Gallium,

Indium, Thallium, Nitrogen, Phosphorus, Arsenic, Antimony, and Bismuth). The potential that is applied to gate 304 in order to deplete the reset channel is increased (i.e. due to the resulting increase in the work function of the gate 304) without having to use high doping levels in the transistor 302.

The source 306 is formed with a p-type well 318, and partially beneath the n-type gate portion 312 of gate 304. The p-type well 318 is diffused into or formed with the substrate 320. The source 306 is preferably formed as a shallow surface implant on the p-type well 318.

The drain 308 is formed with the substrate 320 and partially beneath the p-type region 314 of the gate 304. The drain 308 is electrically associated with a photo-detector 310 that is formed by the deep implant 316 and the drain 308 in the substrate 320. The drain 308 is preferably formed as a shallow surface implant on the deep implant 316 and underlying substrate 320.

The material between the p-well 318 of the source 306 and drain 308 define a length 322 of a channel in the substrate 320. The well portion of the channel constitutes a portion of the p-type well 318 of the source 306. The channel substrate portion has a first conductivity type (e.g. n-type) while the p-well portion 318 has a second conductivity type (e.g. p-type). Therefore, because the p-well portion 318 is disposed away from the drain 308 (i.e. away from the photo-detector 310 side of the transistor), the capacitance typically associated with the p-type well 318 and drain junction in a conventional NMOS FET is effectively removed (i.e. channel substrate portion has the same conductivity type as the drain 308) that substantially suppresses reset noise. In addition, the drain 308 dose may be reduced from $3e^{13}$ cm^{-3} n-type, the

typical level for a conventional NMOS FET, to approximately $2e^{12}$ cm^{-3} n-type since there is no need to overcome the high p-type doping of the p-well 318.

In FIG. 4, a cross sectional view of still another example of an implementation of the sensor 400 having a FET transistor 402 is illustrated. The transistor 402 includes a gate 404, a source 406, a drain 408. The gate 404 has an n-type region 410 and a p-type region 412 overlying dielectric insulator 414. The source 406 includes a p-type well 416 formed in a substrate 418. The drain 408 of transistor 402, however, is formed with a p-type surface implant 420. The p-type surface implant 420 is formed in the drain 408 partially beneath the p-type region 412 of the gate 404, such that the drain 408 is not in direct contact with the surface of gate 404 (i.e., is in contact with the dielectric insulator 414 of the gate 404). The material under the dielectric insulator 414 has a length 422 defined by the separation of the p-type well 416 and drain 408 located beneath the gate 404.

Turning to FIG. 5 is a flow diagram illustrating an example process for resetting the sensor 100 shown in Fig. 2. The process begins 500 when a potential is applied to the gate 108 (FIG. 2), resulting in the channel well portion being depleted 502 (FIG. 5). The drain 110 is not in direct contact with the surface channel of gate 108 due to the insulator 200. The gate 108 forces conduction (i.e. during a reset operation) away from the gate 108 edge nearest the drain 110. Therefore, substantially no conduction occurs through the channel substrate 418 until the potential on the source 106 and the depleted channel p-well portion 204 is sufficient to punch through to the drain 110.

As the applied potential to the gate 108 and the channel well portion is increased during the tapered reset (See FIG. 6 for representative tapered reset voltage waveform). The depletion regions associated with the p-type well 204 of the source

106 and drain 110 merge below the implant 208 to accomplish the punch through of the channel 504 (FIG. 5). Once punch through occurs, carriers are swept through the merged depletion region 506 from the drain 110 to the p-type well 204 of the source 106. In other words, the potential or reset voltage applied to the gate 108 must be increased beyond the level required for the channel well portion to be depleted in order to punch through the substrate 202 portion. Once punch through is accomplished a electrical field is establish to release or diffuse the charge on the photo-detector through the created reset channel. The voltage applied to the gate 108 is reduced allowing the channel below the implant 208 to collapse starting at the drain 110 end of the channel before the source end. Thus, sweeping the charges away from the photo-detector 508. Because there are very few minority carriers in the fully depleted channel, there is reduced thermal noise associated with this charge transfer process. Processing is completed 510 and the photo-detector 102 discharged when the voltage is removed from gate 108.

In FIG. 6, a voltage plot is shown. The reset voltage 600 is applied and then tapered or lowered slowly, preferably over one clock cycle 602, to gradually maintain the potential difference between the channel ends (i.e. between source and drain) such that the charge on the photo-detector is sufficiently removed. As the reset voltage is tapered or lowered, the portion of the channel created by punching through the channel substrate portion is pinched off or collapses before the depleted portion of the reset channel (i.e. the channel well portion) causing charges remaining in the reset channel to be swept towards the source and away from the drain or photo-diode 102.

FIG. 7 is a flow diagram of another example process for resetting the sensor 100 is shown. The process begins 700 with the potential required to deplete a channel

associated with a material between the source 204 (FIG. 2), and the drain 110 under the gate 108 being increased 702. A Boron implant 208 (FIG. 2), is added to half of the reset channel that is nearest the photo-detector 210 during fabrication. The implant raises the surface threshold for creation of a depletion region in the transistor by approximately 0.8 volts or higher. A tapered voltage of FIG. 6 is applied to the gate 108 causing a channel to be created 704 under the implant 208. While the channel exist under the implant 208, a path exist for a charge to flow from the photo detection device, such as a photo-detector 102 or photodiode, to the source 204 and eventually to the reset voltage sink 114 (FIG. 1). Thus, the channel drains the charge 706 from the photo-detector 102 to the p-well 204 of the source 106. Upon removal of the voltage at the gate 202 the channel between the source and drain is interrupted and the process is finished 208.

While various embodiments of the invention have been described, it will be apparent to those of ordinary skill in the art that many more embodiments and implementations are possible that are within the scope of this invention.

CLAIMS

What is claimed is:

1. A sensor having a transistor with a gate located partially over a source and partially over a drain, comprising:

a material between the source and drain beneath the gate having a predetermined length; and

a detection device coupled to the drain by a signal path, wherein the material allows the detection device to be reset to a predetermined state.

2. The sensor of claim 1, further including an implant in the material that increases a surface threshold of the transistor.

3. The sensor of claim 2, wherein the surface threshold of the transistor is increased to at least 0.8 volts.

4. The sensor of claim 2, wherein the implant is in approximately a half of the length of the material.

5. The sensor of claim 3, wherein the half of the material is closest the detection device.

6. The sensor of claim 2, wherein the implant is boron.

7. The sensor of claim 2, wherein the predetermined length of the material is at least 20 percent greater than a process minimum.

8. The sensor of claim 2, wherein the drain is formed by a phosphorous implant level between $3e^{13}$ cm^{-3} and about $6e^{12}$ cm^{-3}.

9. The sensor of claim 2, wherein the gate has a gate length approximately two times a process minimum.

10. The sensor of claim 1, wherein the gate is divided into a p-type region and a n-type region.

11. The sensor of claim 10, wherein the predetermined length of the gate is approximately two times a process minimum.

12. The sensor of claim 10, wherein the material is a p-type material.

13. The sensor of claim 12, wherein the p-type substrate is in proximity to the p-type region of the gate.

14. The sensor of claim 10, wherein the drain is formed by a phosphorous implant level of approximately $2e^{12}$ cm^{-3}.

15. The sensor of claim 10, including an implant region located in the drain extending under the p-type region of the gate.

16. The sensor of claim 15, wherein the implant region is a surface boron implant region.

17. The sensor of claim 1, wherein the detection device is a photo-detector.

18. The sensor of claim 17, wherein the photo-detector is a photodiode.

19. A method for resetting a sensor having a transistor with a gate located partially over a source and partially over a drain, comprising:

increasing a potential that is required in order to deplete a channel associated with a material between the source and the drain under the gate;

depleting the channel between the source and drain in response to a tapered voltage applied to the gate overcoming the potential; and

draining a charge through the transistor from a detection device in response to the creation of the channel.

20. The method of claim 19, wherein increasing the potential further comprises implanting boron in the material between the source and the drain.

21. The method of claim 19, wherein increasing the potential further comprises increasing the surface threshold of the transistor by at least 0.8 volts.

22. The method of claim 19, wherein implanting boron further includes doping a half of the length of the material with boron.

23. The method of claim 22, wherein doping a half of the length of the material occurs in the material closest the detection device.

24. The method of claim 19, wherein creating a channel further includes forming a channel 20 percent greater than a process minimum.

25. The method of claim 19, wherein creating a channel further includes doping the drain with a phosphorus implant level between $3e^{13}$ cm^{-3} and about $6e^{12}$ cm^{-3}.

26. The method of claim 19, wherein increasing the surface threshold level of a material between the source and the drain under the gate further includes dividing the gate into a p-type region and a n-type region.

27. The method of claim 26, wherein the p-type region and the n-type region combined is approximately two time a process minimum in length.

28. The method of claim 26, wherein the p-type region and the n-type region combined in the gate has a gate length approximately two time a process minimum in length.

29. The method of claim 26, wherein increasing the potential further includes creating the drain with a phosphorous implant level of approximately $2e^{12}$ cm^{-3}.

30. The method of claim 26, wherein creating a channel further includes forming an implant region located in the drain extending under the p-type region of the gate.

31. The method of claim 30, wherein the implant region located in the drain contains Boron.

32. A sensor having a transistor with a gate located partially over a source and partially over a drain, comprising:

means for increasing a potential that is required in order to deplete a channel associated with a material between the source and the drain under the gate;

means for depleting the channel between the source and drain in response to a tapered voltage applied to the gate overcoming the potential; and

means for draining a charge through the transistor from a detection device in response to the creation of the channel.

33. The sensor of claim 32, wherein increasing means further comprises means for implanting a hole-increasing dopant in the material between the source and the drain.

34. The sensor of claim 33, wherein implanting means further includes a half of the length of the material being doped with the hole-increasing dopant.

35. The sensor of claim 34, wherein the half of the length of the material occurs in the material closest the detection device.

36. The sensor of claim 34, wherein the hole-increasing dopant is Boron.

37. The sensor of claim 32, wherein the increasing means increases the surface threshold of the transistor by at least 0.8 volts.

38. The sensor of claim 32, wherein the creating means further includes the channel having a channel length that is 20 percent greater than a process minimum.

39. The sensor of claim 32, wherein the creating means further includes means for doping the drain with an electron-increasing dopant implant level between $3e^{13}$ cm^{-3} and about $6e^{12}$ cm^{-3}.

40. The sensor of claim 39, wherein the electron-increasing dopant is Phosphorus.

41. The sensor of claim 32, wherein increasing means further includes means for dividing the gate into a p-type region and a n-type region.

42. The sensor of claim 41, wherein the p-type region and the n-type region combined is approximately two time a process minimum in length.

43. The sensor of claim 41, wherein the p-type region and the n-type region combined in the gate has a gate length approximately two time a process minimum in length.

44. The sensor of claim 41, wherein the increasing means further includes means for creating the drain with an phosphorous level of approximately $2e^{12}$ cm^{-3}.

45. The sensor of claim 41, wherein the creating means further includes means for forming an implant region located in the drain extending under the p-type region of the gate.

46. The sensor of claim 45, wherein the implant region located in the drain contains hole-increasing dopant.

47. The sensor of claim 46, wherein the hole-increasing dopant is boron.

48. The sensor of claim 32, wherein the detection device is a photo-detector.

49. The sensor of claim 48, wherein the photo-detector is a photodiode.

ABSTRACT

A sensor may be formed with a transistor comprising a gate that has both n-type and p-type regions to increase the gate work function. In combination with moving the p-type well such that the p-type well only partially dopes the channel of the transistor, the increased gate work function further increases the reset voltage level required to create the reset channel without having to use high doping levels in the critical regions of the sensor structure including the photo-detector and the reset transistor. The source of the reset transistor is partially beneath the n-type region of gate, while the transistor's drain is partially beneath the p-type region of the gate. The channel has a p-type well portion and a substrate portion. This construction of the sensor may eliminate the reset noise associated with the uncertainty of whether the charge left in the transistor's channel will flow back towards the photo-detector after the transistor has been turned off.

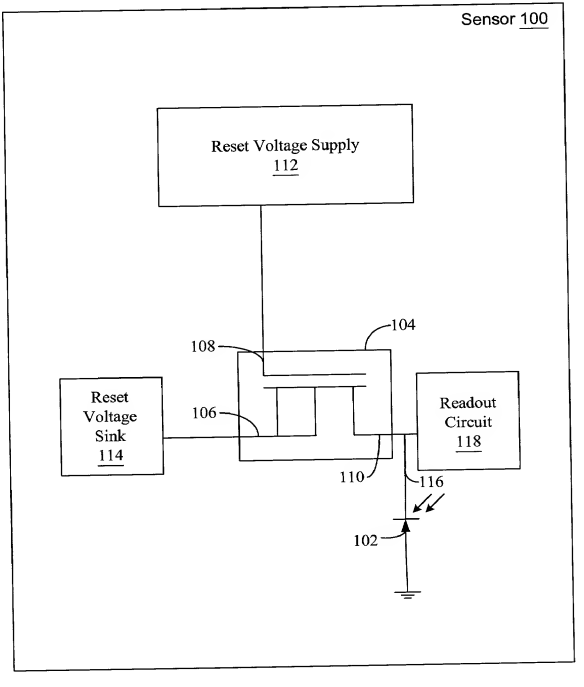
Sensor 100
Reset Voltage Supply
112
104
108
Reset
Voltage
Sink
114
106
Readout
Circuit
118
110
116
102

FIG. 1

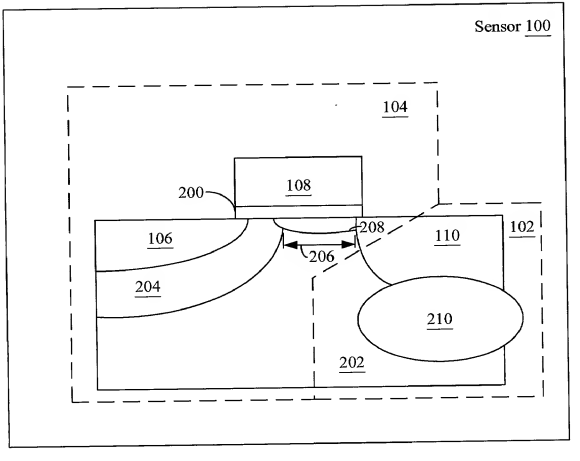

FIG. 2

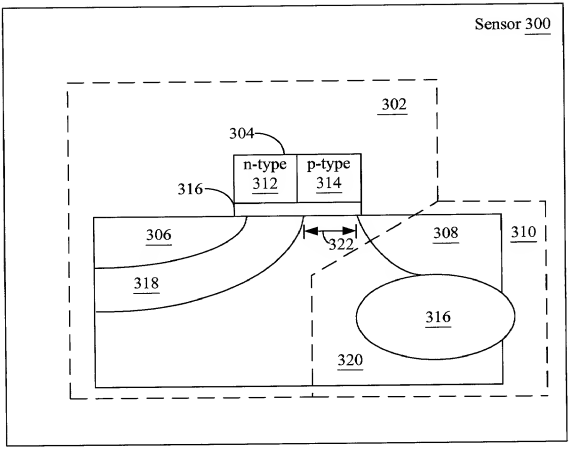
Sensor 300
302
304
n-type
312
p-type
314
316
306
322
308
310
318
316
320

FIG. 3

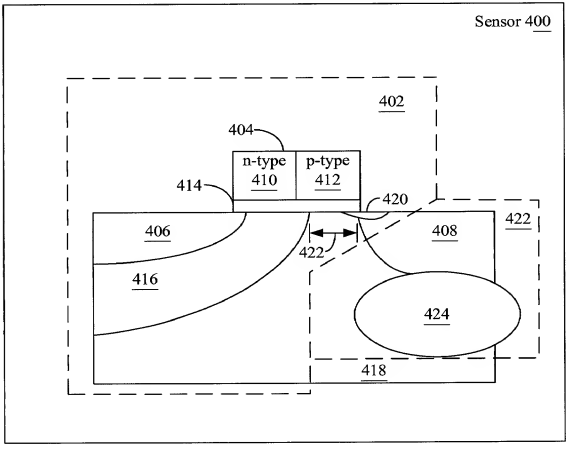
Sensor 400
402
404
n-type
410
p-type
412
414
420
406
422
408
422
416
424
418

FIG. 4

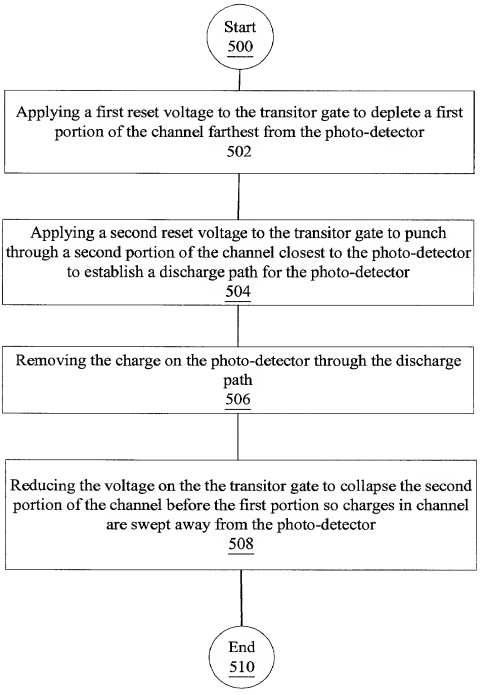
Start
500
Applying a first reset voltage to the transitor gate to deplete a first portion of the channel farthest from the photo-detector
502
Applying a second reset voltage to the transitor gate to punch through a second portion of the channel closest to the photo-detector to establish a discharge path for the photo-detector
504
Removing the charge on the photo-detector through the discharge path
506
Reducing the voltage on the the transitor gate to collapse the second portion of the channel before the first portion so charges in channel are swept away from the photo-detector
508
End
510

FIG. 5

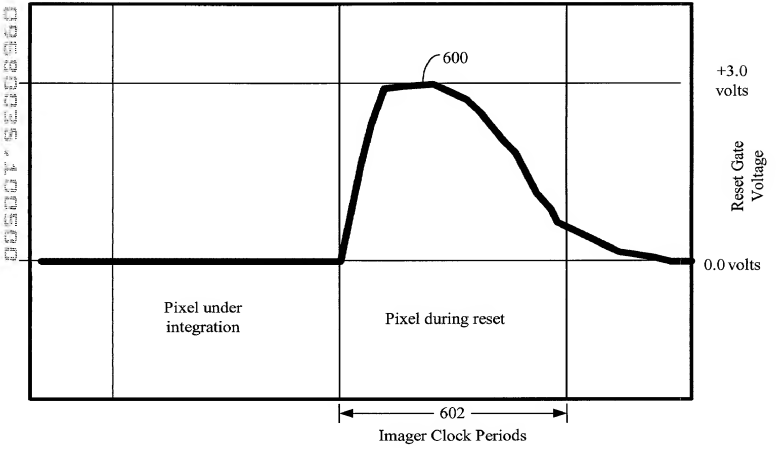
600
+3.0
volts
Reset Gate
Voltage
0.0 volts
Pixel under
integration
Pixel during reset
602
Imager Clock Periods

FIG. 6

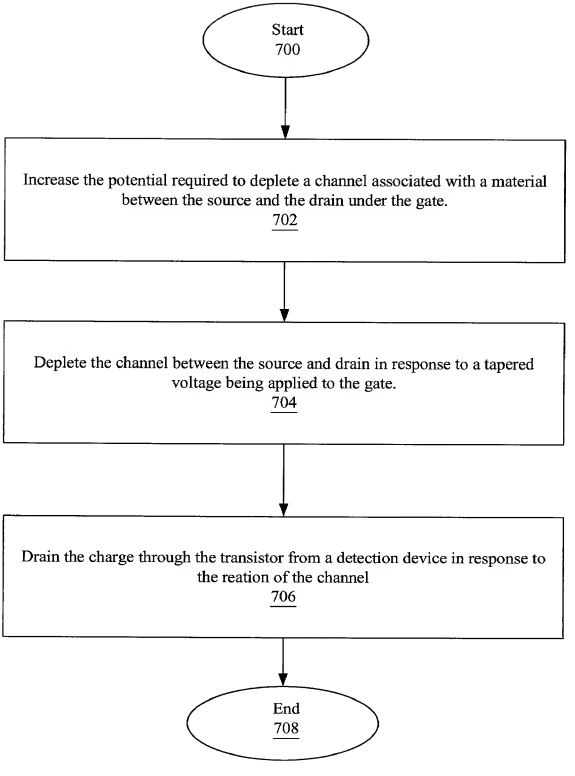
Start
700
Increase the potential required to deplete a channel associated with a material between the source and the drain under the gate.
702
Deplete the channel between the source and drain in response to a tapered voltage being applied to the gate.
704
Drain the charge through the transistor from a detection device in response to the reation of the channel
706
End
708

FIG. 7

PATENT
SNR Matter No.09785980-0021
00CXT0319T

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare:

That my residence, post office address and citizenship are as stated below next to my name.

That I verily believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

the specification of which (check one)
(X) is attached hereto.
( ) was filed on _____ as
Application Serial No. _____
and was amended on _____

That I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

That I acknowledge the duty to disclose information known to be material to patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

That I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) Claimed			Priority
_____ ☐	_____	_____	:
(Number)	(Country)	(Day/Month/Year Filed)	
_____ ☐	_____	_____	:
(Number)	(Country)	(Day/Month/Year Filed)	Yes

No

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

(Application Number) (Filing Date)

(Application Number) (Filing Date)

That I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

United States Application(s)

(Application Serial No.) (Filing Date) (Status)-(Patented, pending, abandoned)

(Application Serial No.) (Filing Date) (Status)-(Patented, pending, abandoned)

That all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

I hereby appoint the following attorneys, with full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith and request that all correspondence and telephone calls in respect to this application be directed to **Francisco A. Rubio-Campos at SONNENSCHEIN, NATH & ROSENTHAL, P. O. Box 061080; Wacker Drive Station, Sears Tower, Chicago, Illinois 60606-1080.**

Attorney	Registration No.	Attorney	Registration No.
Howard B. Rockman	22,190	Jennifer H. Hammond	41,814
Joseph A. Mahoney	38,956	Lana M. Knedlik	42,748
Jordan A. Sigale	39,028	Michael A. Molano	39,777
Francisco A. Rubio-Campos	45,358	Michael L. Kiklis	38,939
Marina N. Saito	42,121	Shashank S. Upadhye	N/A – limited authority
Alison P. Schwartz	43,863	Daniel N. Yannuzzi	36,727
Janelle D. Strode	34,738	James K. Dawson	41,701
Brian J. Gill	P46,727	Kelly H. Hale	36,542
Christopher P. Rauch	45,034	Robert P. Hart	35,184
Kevin W.Guynn	29,927	Keith Kind	42,735
David R. Metzger	32,919	Semion Talpalatsky	35,380
Gregory B. Gulliver	44,138		

Full name of joint inventors: Richard A. Mann

Inventor's signature: Richard A. Mann

Date: 10/3/00

Residence and Post Office Address: 808 Teri Ave
Torrance, California 90503-5118
U.S.A

Citizenship: United States of America

Full name of joint inventors: Lester J. Kozlowski

Inventor's signature:

Date: Oct. 5, 2000

Residence and Post Office Address: 212 Golden Fern Court
Simi Valley, Ventura County,
California 90503-5118
U.S.A

Citizenship: United States of America

Address for Correspondence: **Francisco A. Rubio-Campos**
Sonnenschein Nath & Rosenthal
P. O. Box 061080
Wacker Drive Station
Sears Tower
Chicago, IL 60606-1080